FIG. 1—THIS LEADING-EDGE DETECTOR circuit has a positive output pulse.
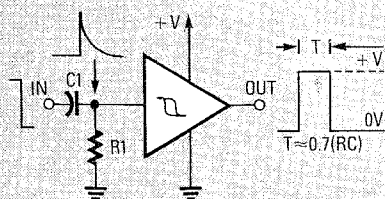
WORKING WITH MONOSTABLE MULTIVIBRATORS

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CIRCUIT DESIGNERS often need to come up with a circuit to generate a pulse when triggered by the leading or trailing edge of a waveform. When the pulse width is not critical, they usually turn to a circuit element that's known as a *half-monostable* or *edge-detector*. When the pulse width is critical, they usually use a circuit element known as a *full-monostable multivibrator*.

There are two types of monostables, standard and retriggerable. In a standard monostable circuit, the arrival of the trigger signal initiates an internal timing cycle that causes the output of the monostable to change state at the start of the timing cycle, and then revert back to the original state on completion of the cycle. Note that once a timing cycle has been initiated, the standard monostable is immune to the effects of subsequent trigger signals until the timing period ends. That type of circuit can be modified by adding a RESET control, so that the output pulse can be terminated or aborted at any time.

In a retriggerable monostable circuit, the trigger signal actually resets the monostable and initiates a new timing cycle even if the trigger signal arrives in the midst of an existing cycle. Thus, the retriggerable monostable's output will stay in its active state as long as new trigger pulses are introduced before the timing cycle ends.

The choice of an IC to implement a pulse generator is usually dictated by economics and convenience, rather than by the actual design requirements. So, if the designer needs a
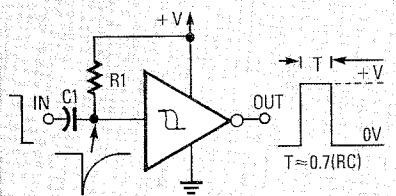

FIG. 2—THIS TRAILING-EDGE DETECTOR circuit also has a positive output pulse.

standard CMOS monostable of only modest precision, he can build it very inexpensively using IC's such as a 4001B or 4011B. Otherwise, it can be done at a greater expense using a 555 timer or a dedicated monostable IC such as 4047B.

Edge-detector circuits

Edge-detector circuits are used to generate an output pulse on the arrival of either the leading or trailing edge of a rectangular input waveform. In most applications, the precise width of the output pulse is not critical. The basic method of making an edge-detector is to feed the input waveform to a short-time-constant RC network, which produces an output waveform with a sharp leading edge and an exponential trailing edge upon the arrival of each input edge. The unwanted edge waveform is then eliminated with a discriminator diode, and the remaining spike or sawtooth waveform is then converted into a clean pulse by feeding it through a Schmitt-trigger.

CMOS Schmitt IC's incorporate built-in protection diodes on all input terminals, which can be used as discriminator diodes as was previous-

Learn how to design and build pulse generators and monostable multivibrators, and how to use them in your projects.
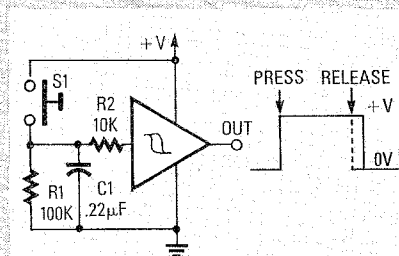

FIG. 3—IF YOU NEED A NOISELESS push-button switch, this circuit can be used to de-bounce a switch.

ly described. The 4093B quad 2-input NOR Schmitt can be used as a normal Schmitt inverter by wiring one input terminal to the positive supply and using the other terminal as the input. Also, a non-inverting Schmitt trigger can be made by wiring two inverting Schmitts in series.

Figure 1 shows a leading-edge detector circuit. The input of the Schmitt is tied to ground via R1, and the RC time constant is relatively short compared to the period of the input waveform. As shown, the leading edge of the input signal is converted to the spike waveform, and the spike is then converted into a pulse waveform by the Schmitt. The circuit will generate a positive-going output pulse if a non-inverting Schmitt is

used, or a negative-going output pulse with an inverting Schmitt. In either case, the output has a period (T) of roughly 0.7(RC). Figure 2 is a similar circuit that is set up as a trailing-edge detector.

An edge-detector circuit can be used to make a "noiseless" push-button switch as shown in Fig. 3. The input of the non-inverting Schmitt is tied to ground via timing-resistor R1 and by input-protection-resistor R2, so the output of the circuit is normally low. When S1 is closed, C1 charges almost immediately to the positive supply voltage, and the Schmitt output goes high. When S1 is released, C1 discharges relatively slowly via R1, and the Schmitt output does not return low until roughly 20 ms later. Therefore, the circuit provides a clean output waveform.

The reset-pulse generator circuit in Fig. 4 generates a reset pulse when power is first applied to the circuit. The circuit produces a 700-ms output pulse for resetting external circuitry. When power is first applied, C1 is discharged, pulling the Schmitt input low and driving the output high. Ca-
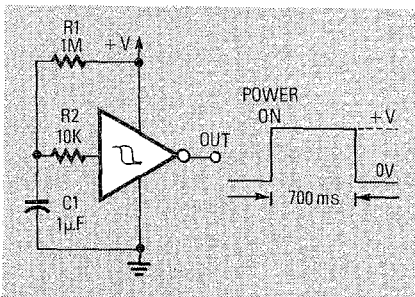
FIG. 4—A RESET-PULSE generator circuit will generate a reset pulse upon power up.

pacitor C1 then charges via R1 until, after about 700 ms, the C1 voltage rises to such a level that the Schmitt output switches low.

Monostable IC's

The cheapest possible way of building a standard or resettable monostable circuit is to use a 4001B quad 2-input NOR gate or a 4011B quad 2-input NAND gate; circuits using those IC's are shown in Figs. 5–8. Note, however, that the output pulse widths of those circuits are subject to variations between individual IC's and variations in the supply voltage, so they are not suitable for use in high-precision applications.

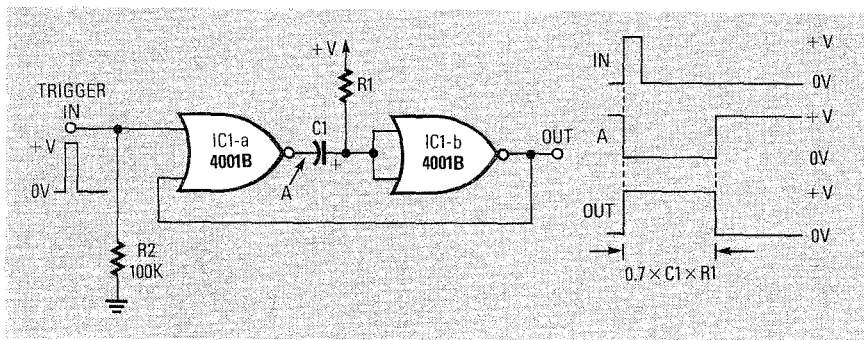Figures 5 and 6 show two versions of the standard monostable circuit,

FIG. 5—THIS 2-GATE NOR monostable is triggered by a positive-going signal and generates a positive-going output pulse.
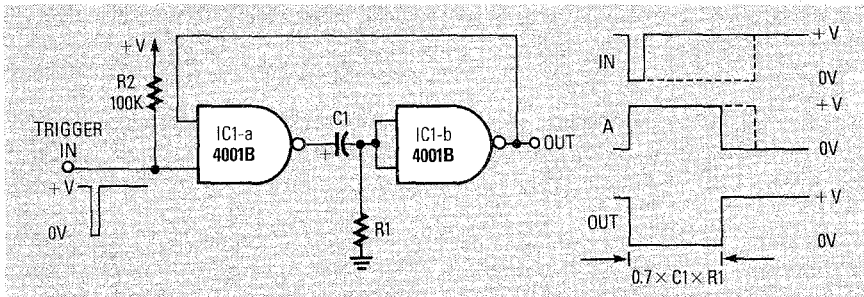
FIG. 6—THIS 2-GATE NAND monostable is triggered by a negative-going signal and generates a negative-going output pulse.
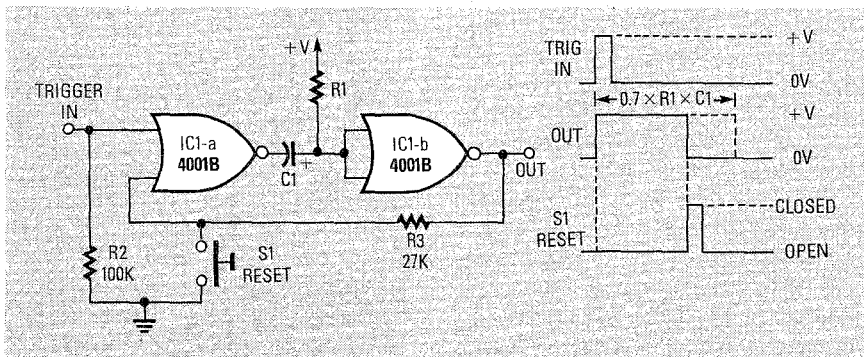
FIG. 7—A RESETTABLE NOR monostable can be reset by pressing S1. It is triggered by a positive-going signal and produces a positive-going pulse.
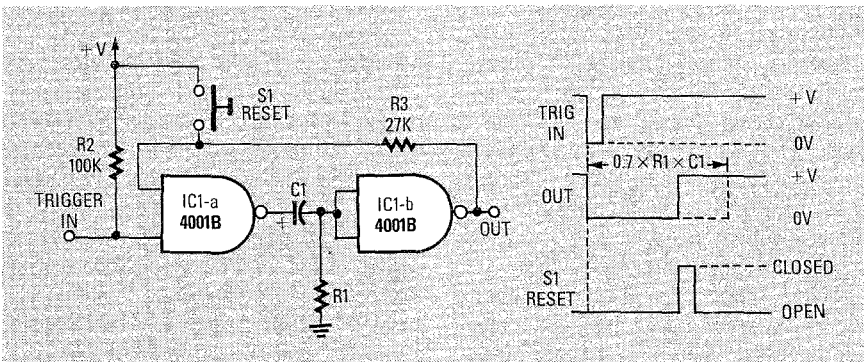
FIG. 8—THE CIRCUIT SHOWN HERE is a NAND monostable. Unlike the NOR-type, it is triggered by a negative-going signal and produces a negative-going pulse.

each using only two of the four gates that are available in the CMOS package. The duration of the output pulse is determined by the values of R1 and C1, and is approximately $0.7 \times C1 \times R1$. When R1 has a value of 1.5 megohms, the period of the pulse is approximately one-second-per-μF of C1's value. In practice, C1 can have any value from about 100 pF up to a few thousand μF, and R1 can have any value from 4.7K to 10 megohms. The NOR version of the circuit (Fig. 5) has a normally-low output, and is trig-

gered by the edge of a positive-going input signal, while the NAND version (Fig. 6) has a normally-high output and is triggered by the edge of a negative-going input signal.

One good feature of those circuits is that the input trigger pulse can be direct coupled, and the duration of the trigger pulse has little effect on the length of the generated output pulse. Another useful feature is that the signal appearing at point A has a period equal to that of either the output pulse or the input trigger pulse, whichever is greater. That feature is valuable when making pulse-length comparators and over-speed alarms.

The operating principles of those two circuits are fairly simple. Let's look first at the circuit in Fig. 5, where IC1-a is wired as a NOR gate and IC1-b is wired as an inverter. When the circuit is in the quiescent stage, the trigger-input terminal is held low by R2, and the output of IC1-b is also low. Both inputs of IC1-a are low, so the output of IC1-a is forced high and C1 is discharged. When a positive trigger signal is applied to the circuit, the output of IC1-a is immediately forced low and, since C1 is now discharged, it pulls the input of IC1-b low and drives its output high. The output of IC1-b is coupled back to the input of IC1-a, and forces the output of IC1-a to remain low, irrespective of the prevailing state of the input trigger signal. As soon as the output of IC1-a switches low, C1 starts to charge up via R1, and after a delay determined by the values of those components, C1's voltage rises to such a level that the output of IC1-b starts to swing low, terminating the output pulse. The circuit will not return to its quiescent state if the trigger signal is high when the output pulse is terminated.

The circuit in Fig. 6 operates like the one in Fig. 5, except that IC1-a is
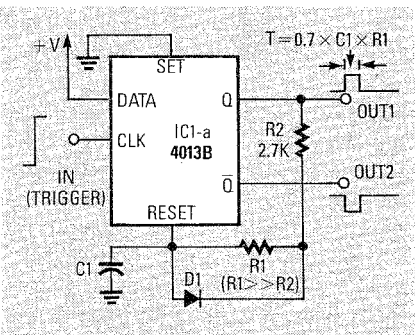

FIG. 9—A D-TYPE FLIP-FLOP can be used as a monostable. It produces both negative- and positive-going pulses.
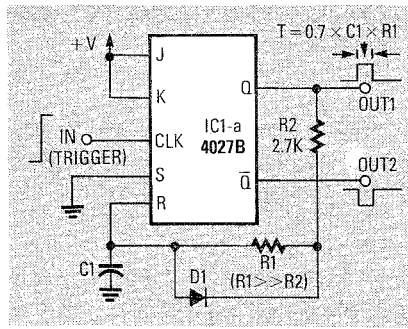

FIG. 10—A JK-TYPE FLIP-FLOP can also be used as a monostable. Its operation is similar to the D-type in Fig. 9.
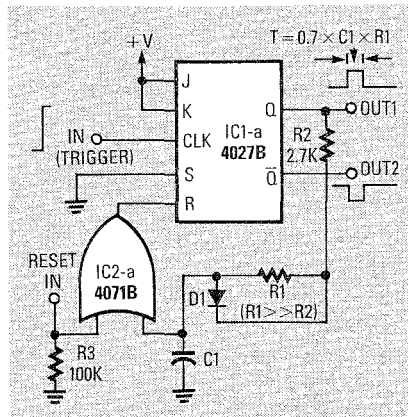

FIG. 11—THIS JK-TYPE monostable is electronically resettable.
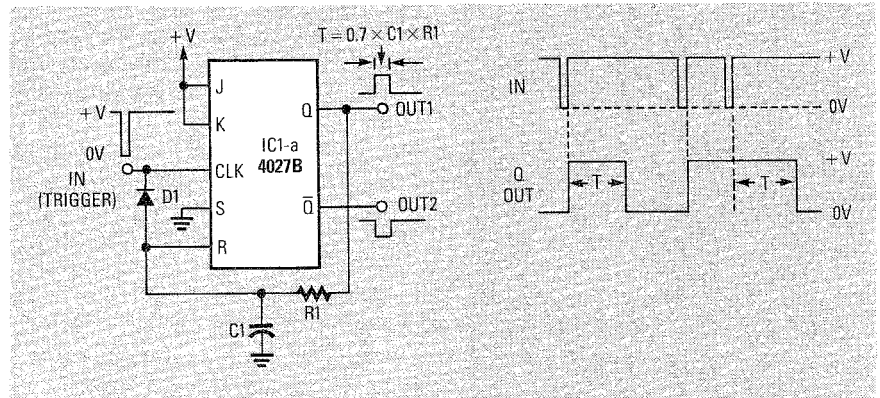

FIG. 12—A RETRIGGERABLE JK-type monostable has an output pulse that can be prolonged by an additional trigger pulse before the timing cycle ends.

wired as a NAND gate, with its trigger input tied to the positive supply via R2, and the timing-resistor R1 is connected to ground.

The circuits in Figs. 5 and 6 have their outputs coupled directly to one input of IC1-a to effectively maintain a trigger input once the original trigger signal is removed, thereby providing semi-latching operation.

The circuits in Figs. 5 and 6 can be made resettable by providing them with a means of breaking the feedback path, as shown in Figs. 7 and 8. The feedback connection from the output of IC1-b to the input of IC1-a is made

via R3. Consequently, once the circuit has been triggered, and the original trigger signal has been removed, the circuit can be reset by forcing the feedback input of IC1-a to its normal quiescent state by pressing S1. In practice, S1 can be replaced with a transistor, enabling the circuit to be reset electronically.

Flip-flop monostables

Medium-accuracy monostable circuits can be built using standard edge-triggered CMOS flip-flop IC's, such as the 4013B dual D-type or the 4027B dual JK-type, in the configurations shown in Figs. 9 and 10. Both circuits operate in the same basic manner, with the IC wired in the divider mode by proper connection of their control terminals (DATA and SET in the 4013B, and J, K and SET in the 4027B), but with the Q terminal connected to RESET by an RC time-delay network. The operating sequence of both circuits is as follows:

When the circuit is in its quiescent state, the Q output terminal is low and discharges timing capacitor C1 via R2 and the parallel combination of R1 and D1. Upon the arrival of a sharply rising leading edge on the CLK terminal, the Q output flips high, and C1 starts to charge up via the series combination of R1 and R2. Eventually, after a delay determined mainly by values of C1 and R1, the C1 voltage rises to such a value that the flip-flop is forced to reset, driving the Q terminal low again. Capacitor C1 then discharges rapidly via R2 and the D1/R1 network, and the circuit is ready to generate another output pulse when the next trigger signal arrives.

The timing period of the circuits in Figs. 9 and 10 is roughly equal to 0.7 × C1 × R1, and the reset period (the

time for C1 to discharge after each pulse) is roughly equal to C1 × R2. In practice, R2 is used mainly to prevent degradation of the trailing edge of the pulse waveform as C1 discharges; R2 can be replaced by a jumper if degradation is acceptable. Note that the circuit generates a positive-going output pulse at Q, and a negative-going pulse at $\overline{Q}$.

The circuit in Fig. 10 can be made resettable as shown in Fig. 11. That is done by connecting capacitor C1 to the RESET terminal of the circuit via one input of an OR gate, and using the
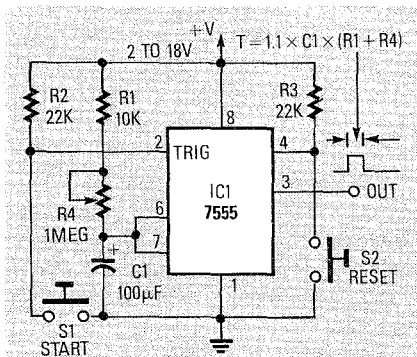

FIG. 13—THIS MONOSTABLE can be manually-triggered and has a variable pulse width from 1.1 to 100 seconds.
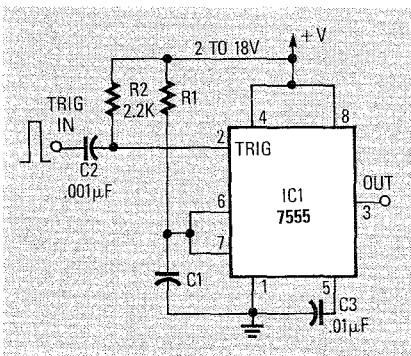

FIG. 14—THIS 7555 MONOSTABLE is similar to the one in Fig. 13, with the exception that it can be electronically triggered.
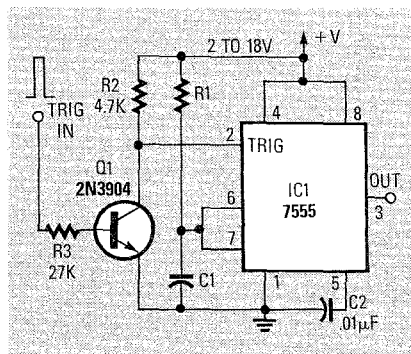

FIG. 15—A PULSE-TRIGGERED 7555 monostable can produce an accurate output pulse from a medium-accuracy input signal.

other input of the OR gate to accept the external reset signal.

Finally, Fig. 12 shows how the 4027B can be used to make a retriggerable monostable, in which the pulse period restarts each time a new trigger signal arrives. Note that the input of that circuit is normally high, and that the circuit is actually triggered on the trailing (rising) edge of a negative-going input pulse. The circuit operates as follows:

At the start of each timing cycle, the input trigger pulse switches low and rapidly discharges capacitor C1 via D1 and shortly afterwards, the trigger pulse switches high again, releasing C1 and simultaneously flipping the Q output high. The timing cycle then starts in the normal way, with C1 charging via R1 until the C1 voltage rises to such a level that the flip-flop resets. That drives the Q output low again and C1 slowly discharges via R1. If a new trigger pulse arrives in the midst of a timing period (when Q is high and charging C1 via R1), C1 rapidly discharges via D1 on the low part of the trigger, and commences a new timing cycle as the input waveform switches high again. In practice, the input trigger pulse must be wide enough to fully discharge C1, but should be narrow relative to the output pulse. The timing period of the output pulse equals 0.7 × C1 × R1, and for best results, R1 should have as large a value as possible.

High accuracy monostables

In all of the circuits that we've looked at so far, the width of the output pulse depends on the switching threshold of the IC, which is subject to considerable variation between individual IC's, and variations in supply voltage and temperature. Therefore, the circuits have only moderate accuracy. If precise pulse widths are needed, the best way of generating them it is to use a 7555 IC, which is the CMOS version of the ubiquitous 555 timer. It has a built-in precision voltage comparator that activates internal flip-flops and precisely controls the output pulse width, irrespective of wide variations in supply voltage and temperature. The 7555 can operate from supplies that range from 2 volts to 18 volts.

Figure 13 shows the basic way of using the 7555 as a manually triggered variable-pulse generator. The IC is triggered by briefly pulling pin 2
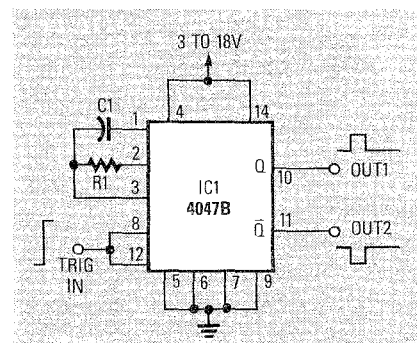

FIG. 16—THE 4047B can be used as a retriggerable monostable, with positive-edge triggering.
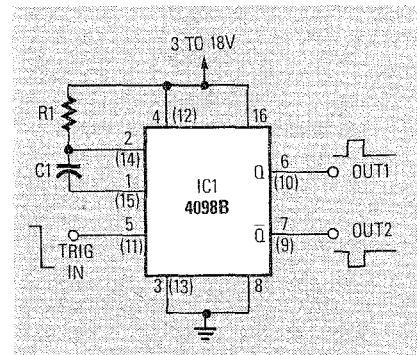

FIG. 17—THE 4098B is used here as a retriggerable monostable with negative-edge-triggering.

low (less than ⅓V) via S1. At that time, the output (pin 3) switches high and the IC enters its timing cycle, with C1 charging up via the R1/R4 circuit. Eventually, after a delay of 1.1 × C1 × (R1 + R4), C1's voltage rises to the upper switching threshold (⅔ V), and the output abruptly switches low, ending the timing cycle. The timing cycle can be terminated prematurely by briefly pulling RESET (pin 4) low via S2. The circuit can produce a pulse from 1.1 to 100 seconds; the duration is controlled by R4.

In most practical applications using the 7555 the designer will want to trigger the IC electronically, rather than manually (by pressing a button). If that's the case, the trigger signal must switch from an off value greater than ⅔V to an on value less than ⅓V (triggering actually occurs as pin 2 drops through the ⅓V value). The pulse width must be greater than 100 ns, but less than the desired output pulse, so that the trigger pulse is removed before the timing period ends.

One way of generating a trigger signal from a rectangular input is to connect the signal to pin 2 of the 7555 via a short-time-constant RC dif-

alignment-tool or a non-conducting screwdriver until the LED glows brightly without flicker, and the voltage at test point TP2 is between 6 and 10 volts. If you have problems with the above procedure, perform the following tests:

● Using an oscilloscope, observe the square-wave output at IC1 pin 3; it should be *clean* with no jitter, as shown in Fig. 5. Overcoupling of the antenna to the TV will cause too much signal on IC1 pin 2, which will result in an unstable output.
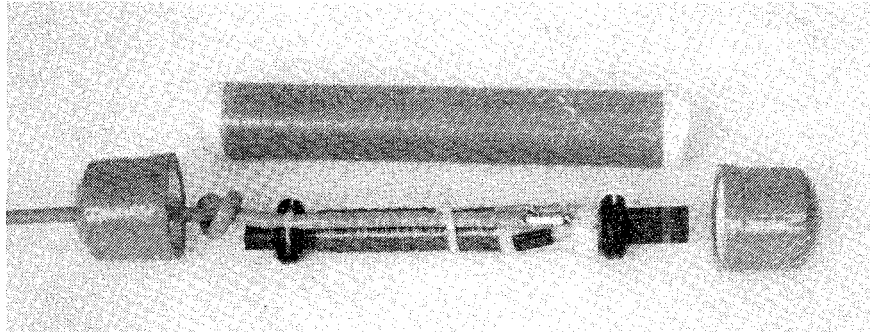

FIG. 4—THE ANTENNA IS HOUSED in a section of PVC pipe. Note that one end cap must be pre-installed on the antenna's connecting cable.

● Check the operation of IC8 by temporarily jumping pin 9 to pin 16. The VCO output at IC8 pin 4 should be greater than 1 MHz but not greater than 1.1 MHz. Reducing the value of resistor R5 will increase the operating frequency.

● Remove the jumper and check IC8 pin 1 for a narrow negative pulse that indicates the PLL is locked. Connect a frequency counter through a ×10 probe at test point TP1 and adjust C10 for a reading of 3579545 Hz when 6 volts is applied to TP2 from an external power supply. In some cases, the value of C9 will need to be changed
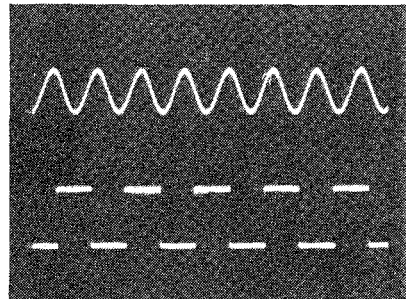

FIG. 5—THE FREQUENCY-STANDARD OUTPUT (bottom trace) should be jitter free. The top trace is the input from the antenna.

slightly to allow a proper adjustment range for C10.

● Connect a frequency counter or a scope to output jack J2 and verify proper operation of the decade counters and wiring of the frequency output select switch. The output level of the standard is adjustable between 0 and 12 volts.

Accuracy

You may have noticed that the readings on your frequency counter may not be exactly 1.000 MHz when the output selector is set for 1 MHz. The worst-case error measured when the TV was tuned to a locally-originated TV program was 1-ppm (*part per million*), or 1 Hz at 1 MHz. When the TV is tuned to a network-originated program the error is less than 1 part in 10^{-7}, or 0.1 Hz at 1 MHz. (The local broadcasts are not always on the network atomic standard. Local news and local live productions use their own master oscillator.)

Set S1 for a 3.58-MHz output and select a network-originated broadcast. Then change the channel to a different network broadcast and note that the reading on the frequency counter is the same—you are thereby assured that the atomic standard is in use. Adjust the counter's timebase to exactly 3579545.45 Hz. If your frequency counter has an external timebase input you can use the 1-second (1-Hz) or the ¹⁄₁₀-second (10-Hz) output from the standard to gate the counter for good accuracy without having to calibrate the counter or warm up its crystal oven (if it has an oven).

The internal decade counters can be reprogrammed to divide by any number between 2 and 10, which makes a myriad of other output frequencies available to those wanting to customize the standard.   **R-E**

ferentiating network. It converts the leading or trailing edge of the input waveform into suitable trigger pulses, as shown in Fig 14.

The best way of triggering the 7555 is to use one of the previously described medium-accuracy monostables to generate a narrow (about 100 ns) positive-going trigger pulse, and transistor-couple it to pin 2 of the 7555, as shown in Fig. 15. Note in that circuit, and also the previous one, C2 is used to decouple the trigger circuitry from supply transients.

CMOS monostables

A number of dedicated CMOS monostable IC's are available. The best of those devices are the 4047B monostable/astable IC and the 4098B dual monostable. It should be noted that both devices have rather poor pulse-width accuracy and stability. They are, however, quite versatile, and can be triggered by either the positive or the negative edge of an input signal, and can be used in the standard or the retriggerable mode.

When the 4047B is used in the monostable mode, the trigger signal actually starts the astable and resets the counter, driving its Q output high. After a number of astable cycles, the counter flips over and simultaneously switches the Q output low. Consequently, the circuit will produce relatively long output pulses; the period is approximately $2.5 \times R1 \times C1$.

In practice, R1 can have any value from 10K to 10 megohms, and C1 must be non-polarized with a value greater than 1000 pF. Figure 16 shows how to connect the 4047B in the retriggerable mode. It can be reset at any time by pulling pin 9 high.

The 4098B dual monostable has two sections that share common supply connections, but can otherwise be used independently. The timing period of both monostables is controlled by a single resistor (R1) and capacitor (C1), and is approximately $0.5 \times R1 \times C1$. Resistor R1 can have any value from 5K to 10 megohms, and C1 can have any value from 20 pF to 100 μF. Figure 17 shows the 4098B used as a retriggerable monostable that is triggered by a negative input edge.   **R-E**